

In the Claims:

Cancel Claims 1-14 without prejudice.

Add the Following New Claims 15-34:

1 Claim 15. A device for matching patterns against data comprising:
2 a first memory in which a set of patterns are stored;
3 a second memory that stores mask data identifying patterns in the first memory
4 to be matched against the data; and
5 pattern match logic circuit arrangement correlating marked patterns in said first
6 memory against the data and generating at least one control signal if a match occurs.

1 Claim 16. The device of Claim 15 wherein the marked patterns are fewer than the total
2 number of patterns in said first memory.

1 Claim 17. The device of Claims 15 or 16 wherein the data is received from a network.

DI 1 Claim 18. The device of Claim 15 or 16 wherein the pattern match logic circuit
2 arrangement includes a first state machine for assembling data received from a network
3 into predetermined sizes and identifying beginnings and endings of data frames; and
4 a second state machine operatively coupled to the first state machine, said
5 second state machine including circuit that receives the predetermined sizes from the
6 first state machine and circuit that generates addresses for accessing the first memory
7 and the second memory, whereat pattern and mask data are to be read and used with
8 the predetermined sizes in generating the first control signal.

1 Claim 19. A method comprising the acts of:
2 providing in a first memory a set of patterns;
3 providing in a second memory mask data identifying patterns in the first memory
4 to be matched against data received from a network;
5 correlating the data against the marked pattern and generating a control signal if
6 a marked pattern matches the data.

1 Claim 20. The method of Claim 19 wherein marked patterns are fewer than the set of
2 ~~patterns.~~

1 Claim 21. A network interface card including:
2 a system interface circuit arrangement;
3 a network interface circuit arrangement;
4 a first storage that stores a set of patterns;
5 a second storage that stores mask data identifying patterns in the first storage to
6 be matched against data; and
7 a pattern match logic circuit arrangement correlating marked patterns in said first
8 storage with the data and generating at least one first control signal if a match occurs
9 between one of the marked patterns and the data.

1 Claim 22. The network interface card of Claim 21 wherein the data is received from
2 the network.

1 Claim 23. The network interface card of claims 21 or 22 further including a host
2 computer coupled to the system interface, said host computer including software for
3 downloading to the network interface card the set of patterns and the mask data.

1 Claim 24. The network interface card of claims 21 or 22 further including address
2 match function logic circuit for correlating an address for the network interface card and
3 a received address and generating a second control signal on the occurrence of a
4 match.

1 Claim 25. The network interface card of claims 21 or 22 wherein each pattern in the
2 set of patterns are arranged in 4 (four) bytes wide words and 128 byte sectors.

1 Claim 26. The network interface card of claim 25 wherein the patterns are arranged
2 contiguously in the Pattern Storage.

1 Claim 27. The network interface card of claim 25 wherein the mask data is arranged
2 so that each M-bits word of mask contains mask bits for words in N patterns, wherein
3 $M = \text{number of bits in a mask word}$ and $N = \text{number of patterns}$.

1 Claim 28. The network interface card of claim 27 wherein $M = 32$ and $N = 8$.

1 Claim 29. The network interface card of claim 21 wherein the pattern match logic
2 circuit arrangement includes a first state machine for assembling data received from the
3 network interface circuit arrangement into predetermined sizes and identifying
4 beginnings and endings of data frames; and

5 a second state machine operatively coupled to the first state machine, said
6 second state machine including circuit that receives the predetermined sizes from the
7 first state machine and circuit that generates addresses for accessing the pattern
8 storage and mask storage, whereat data are to be read and used with the
9 predetermined sizes in generating the first control signal.

1 Claim 30. The network interface card of claim 29 wherein the address generation
2 circuit uses the expression YYYxxxxx to determine the addresses for the Pattern RAM,
3 wherein xxxxx represents an index count and YYY represents states for a state
4 machine.

1 Claim 31. The network interface card of claim 21 wherein the system interface circuit
2 arrangement includes a PCI Interface.

1 Claim 32. The network interface of claim 21 wherein the network interface circuit
2 arrangement includes Ethernet MII Interface.

1 Claim 33. A pattern matching method including the steps of:

- 2 (a) providing a set of patterns;
3 (b) providing data to be matched with selected patterns in said set of
4 patterns;
5 (c) providing pointers for identifying the selected patterns;
6 (d) correlating the data with the selected patterns in step (c); and
7 (e) generating a Match signal if the data of step (d) and the selected patterns
8 match.

1 Claim 34. A method for using in a communications network to wake station connected
2 to the communications network said method including the steps of:

- 3 (a) providing, on a network interface card, multiple patterns against which
4 data from the communications network is to be matched;
5 (b) providing mask data indicating the patterns to be used;
6 (c) correlating each identified pattern with data received from the
7 communications network; and
8 (d) generating a Wake-Up signal if a match occurs in step (c).